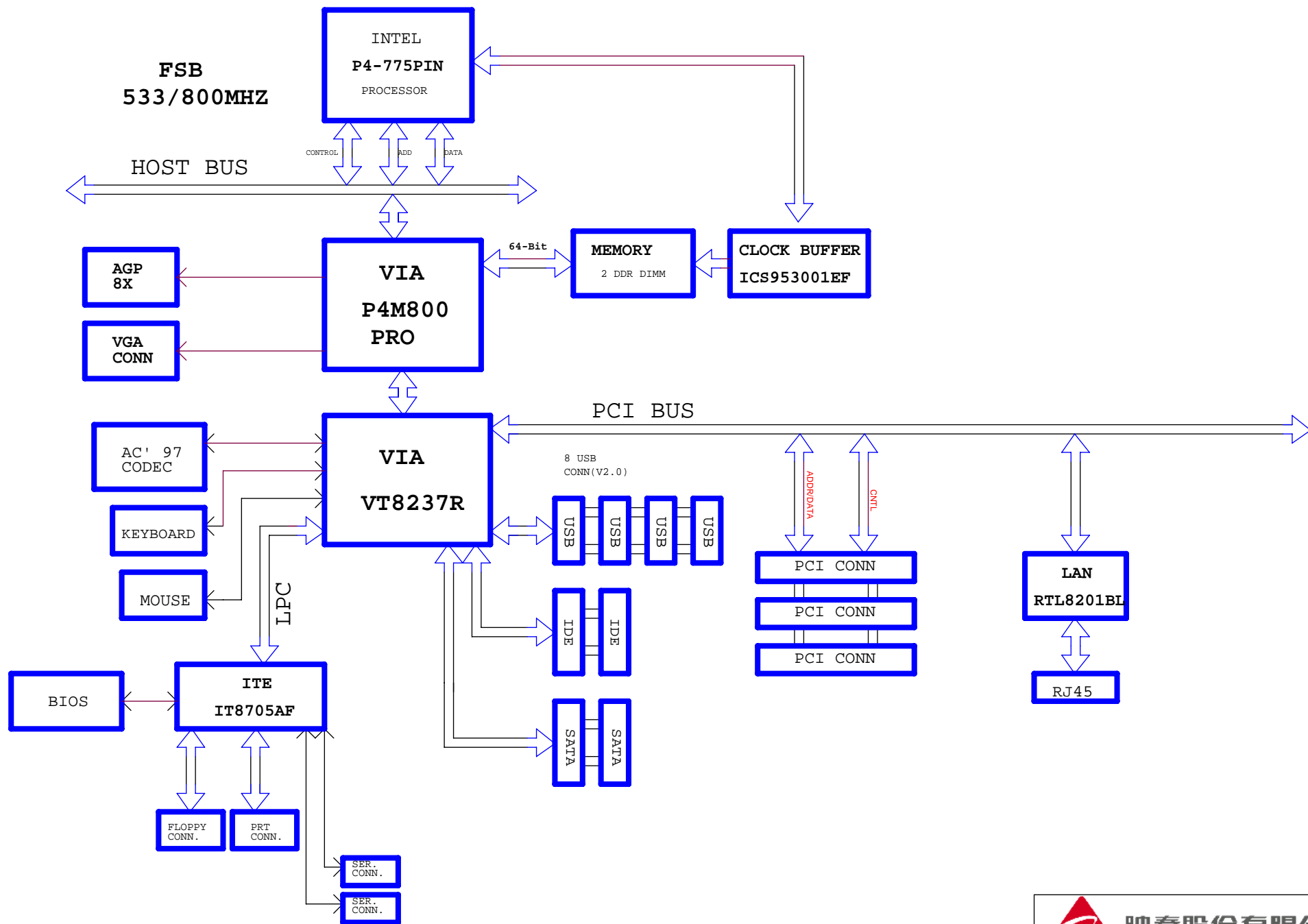


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P4M8P-M7A ***P4M800 PRO +*** ***VT8237R*** ***VER : 1.2***



PCI Solt	IDE SEL	INT#	GNT#	REQ#	CLOCK
1	19	A	0	0	PCLK5
2	20	B	1	1	PCLK0
3	21	C	2	2	PCLK1
4					
5					
6					

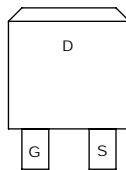
P4M80-M7

1. CPU --- INTEL P4 Socket 775(3-Phase Power)
2. CHIPSET --- VIA P4M800 CE PRO+ VT8237R
3. MEMORY --- 2 DDR SDRAM(Max. 2GB)
4. SLOTS --- AGP(8X)x1, PCIX3, CNRx1
5. CODEC --- Realtek ALC655 6-Channel Audio
6. LAN --- VT6103L
7. PCB Size --- 2438.4Mmx201.68mm, 4-Layer

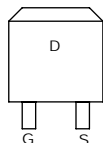
Chips	IDE SEL	INT#	GNT#	REQ#	CLOCK
LPC I/O					PCLK3
LAN					
RAID					
S ATA					
WIRE LESS					
CARD READER					
S / B					SPCLK
AT123S					

SLOT	GPIO	PRI.	SEC.
AMR			
CNR			
ACR			
H/W SOUND			

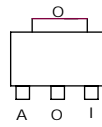
220U/25DE	5*7 mm
100U/16DE	6.3*11 mm
220U/10DE	6.3*11 mm
470U/16DE	8*11 mm
1000U/10DE	8*14 mm
1500U/16DE	10*25 mm
3300U/25DE	10*25 mm



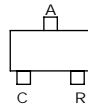
TO-263
PHB55N03
90N02



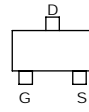
TO-252
20N03
TM3055TL-S
PHD55N03



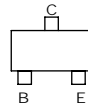
SOT-223
AMS1117



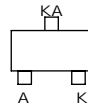
SOT-23
LM431



SOT-23
2N7002
SI2303S
SI2301S



SOT-23
2N3904
2N3906
MMBT2907A
2N2222A



SOT-23
BAT54C
BAT54S




TO-92
LM431
78L05-D
LM432

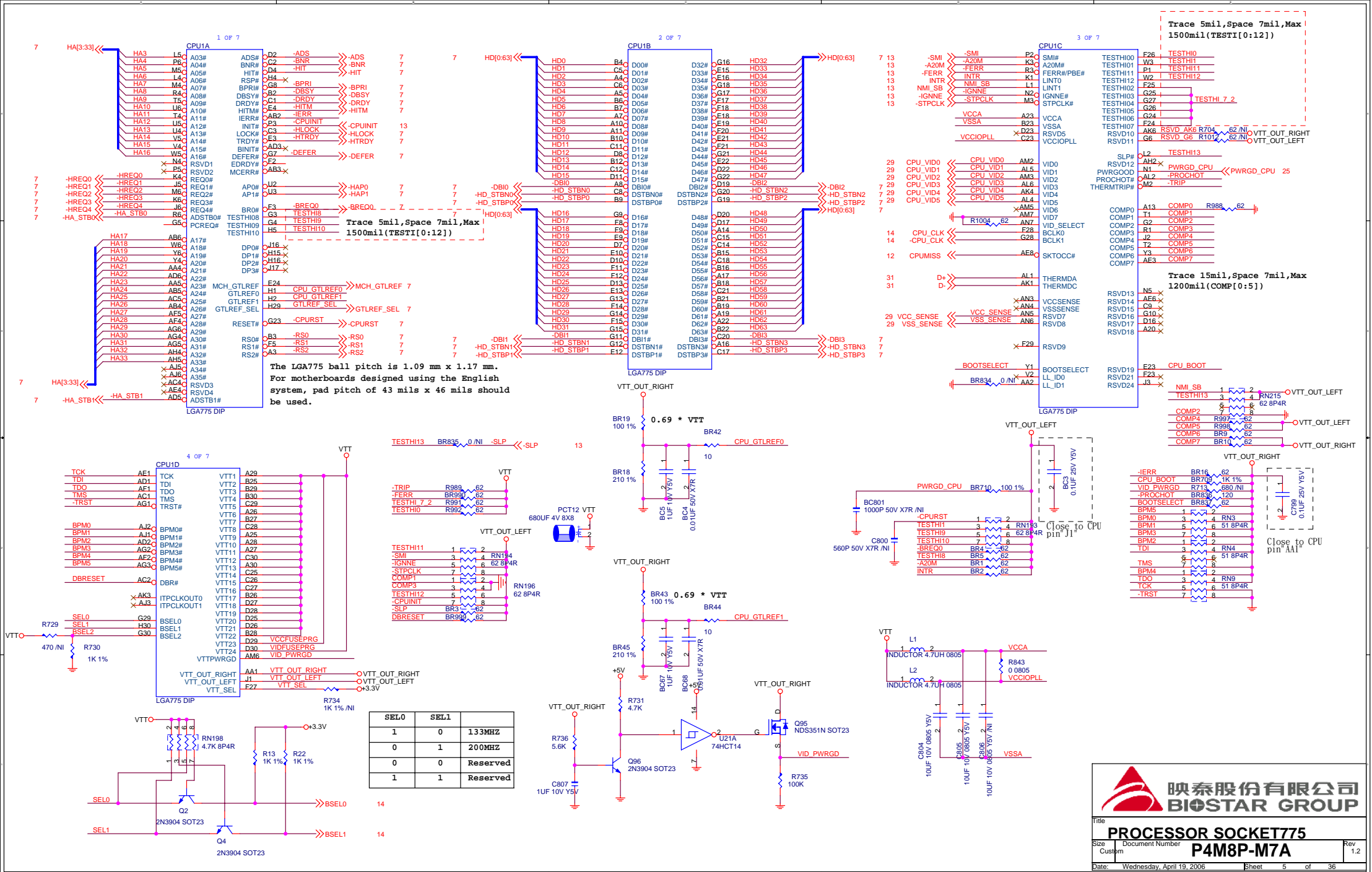


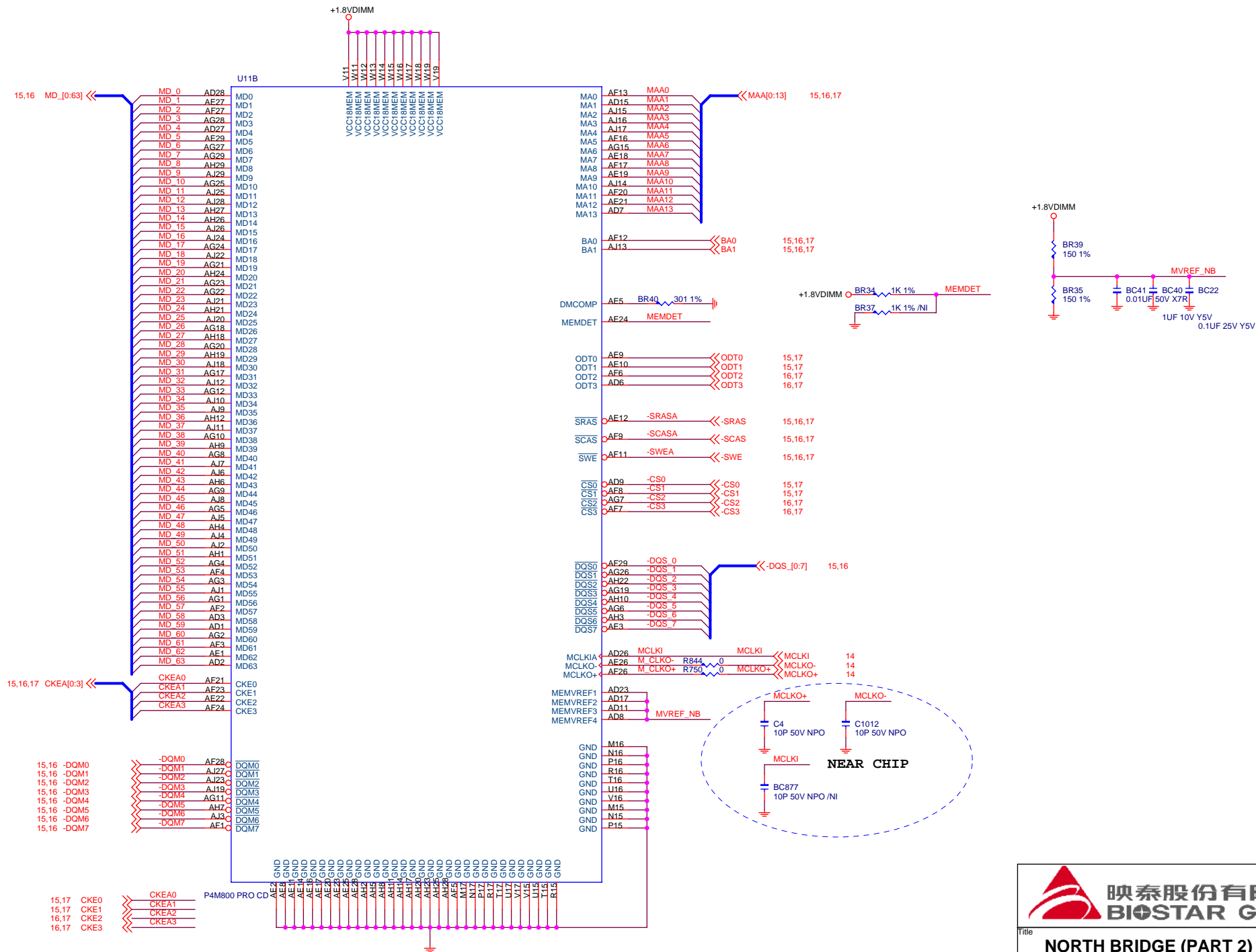
TO-92
2N2222A
2N2097A

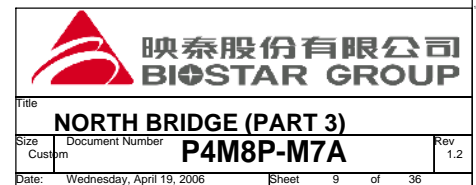


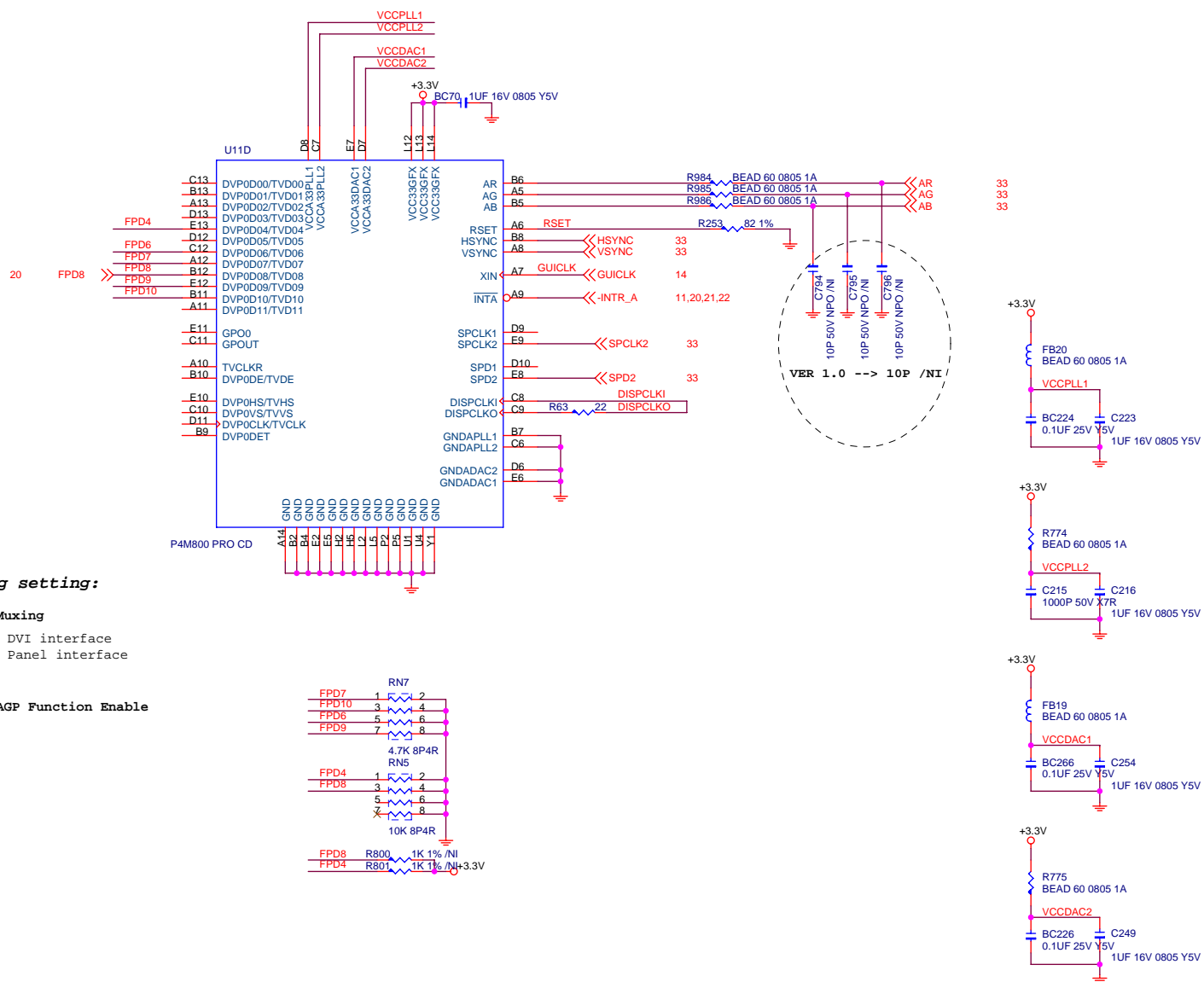
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HSD882-D

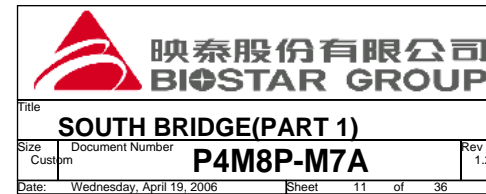
 映泰股份有限公司 BIOSSTAR GROUP		
Title		
GENERAL SPEC		
Size	Document Number	Rev
Custom	P4M8P-M7A	1.2
Date:	Tuesday, April 18, 2006	Sheet 3 of 36











NB STRAPPING FOR PT880/PM880

PD_A0	GPIOA	GPIOC	Host	Clock
0	0	0	100Mhz	
0	0	1	133Mhz	
0	1	1	166Mhz	
0	1	0	200Mhz	
1	0	0	266Mhz	
1	1	1	AUTO Mode	

GPIOB	IOQ Depth
0	12 Level
1	1 Level

GPIOB	GTL pullup
0	Enable
1	Disable

ACSDO R472 4.7K 0/+3.3V
R461 4.7K

0/1:Enable/Disable auto reboot for VT8237

ACSYNC R467 4.7K 0/+3.3V

0/1:Enable/Disable LPC FW command for VT8237

R421 4.7K SEEDI 13

0/1:Disable/Enable LPC shadow EEPROM

SPEAK R434 1K 1% 0/+3.3V

0/1:Enable/Disable CPU FREQ strapping

-PCISTP

0/1 : Enable/Disable 100MHz VLink clock

SMBCK2 LOW

SMBCK2 HIGH

無S3

SMBBDT2 LOW P4M800 Pro

SMBCK2 HIGH P4M800

13

31

FOR EMI

C1018 0.1UF 25V Y5V

25MHZ 20PF 30PPM

15P 50V NPO

15P 50V NPO

25MHZ 20PF 30PPM

15P 50V NPO

15P 50V NPO

25MHZ 20PF 30PPM

15P 50V NPO

15P 50V NPO

25MHZ 20PF 30PPM

15P 50V NPO

15P 50V NPO

25MHZ 20PF 30PPM

15P 50V NPO

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25MHZ 20PF 30PPM

15P 50V NPO

15P 50V NPO

25MHZ 20PF 30PPM

15P 50V NPO

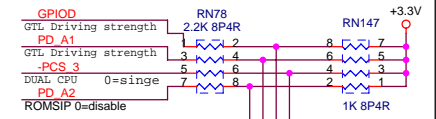
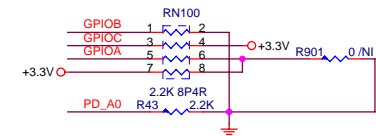
15P 50V NPO

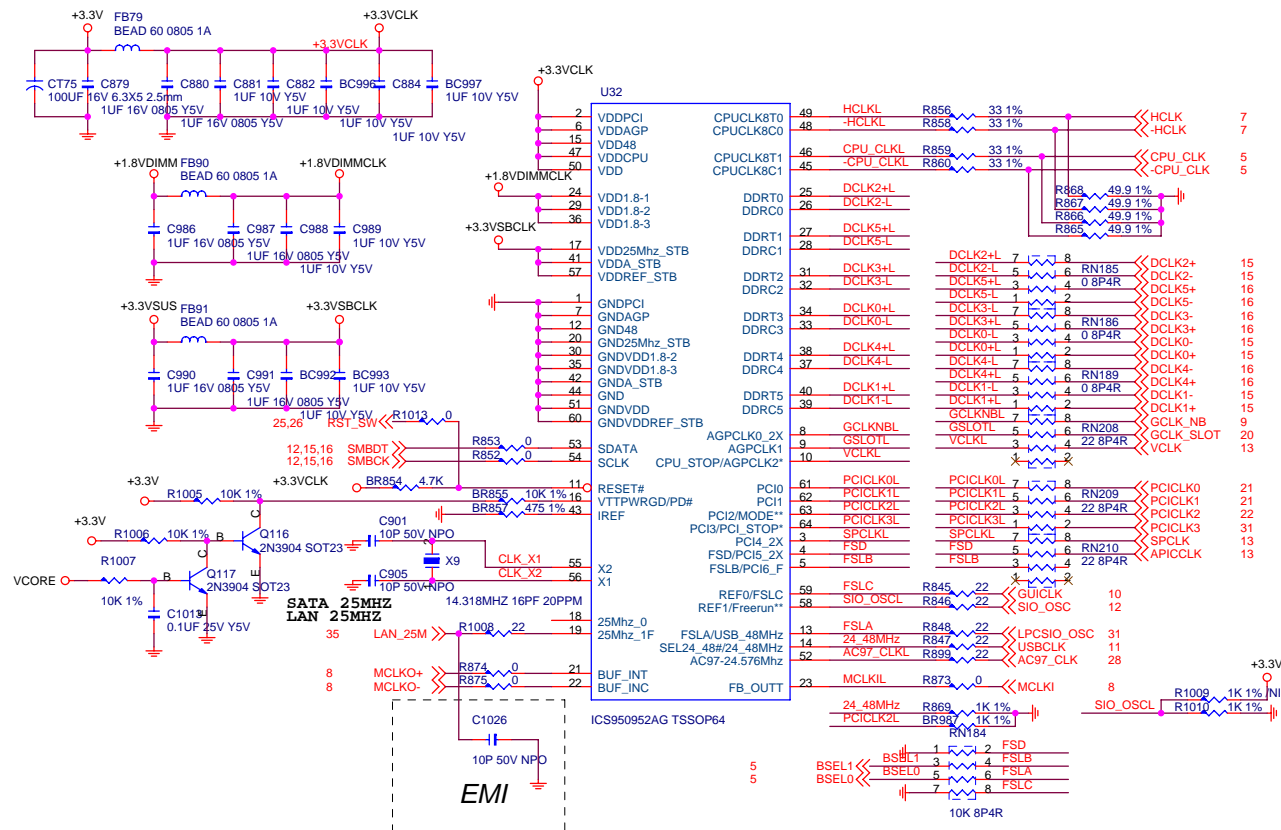
25MHZ 20PF 30PPM

15P 50V NPO

15P 50V NPO

25MHZ 20PF 30PPM



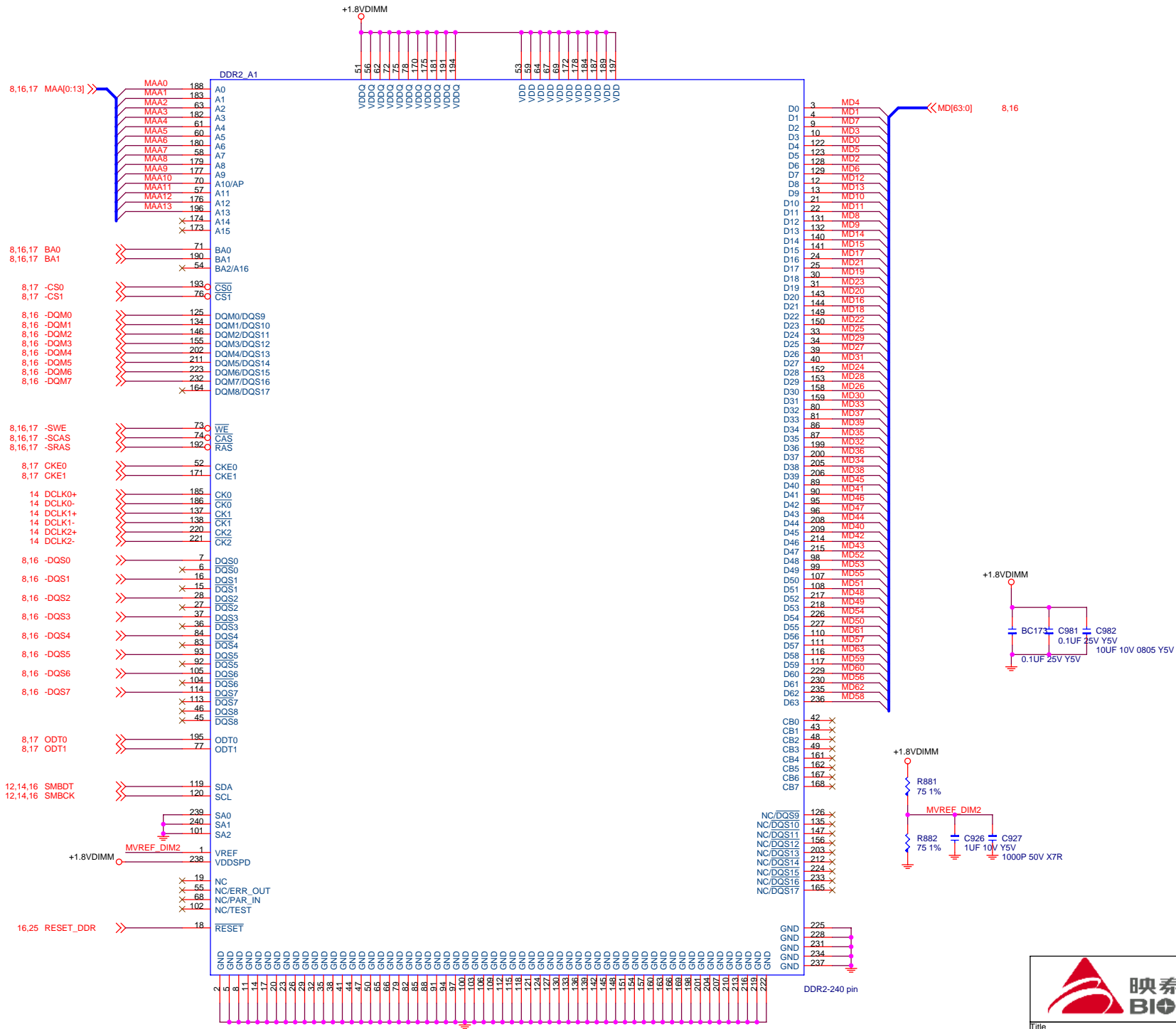


	FSD	FSLC	FSLB	FSLA	CPU	PCI
0	0	0	0	0	266	33
0	0	0	0	1	133	33
0	0	0	1	0	200	33
0	0	0	1	1	166	33
0	1	0	0	0	333	33

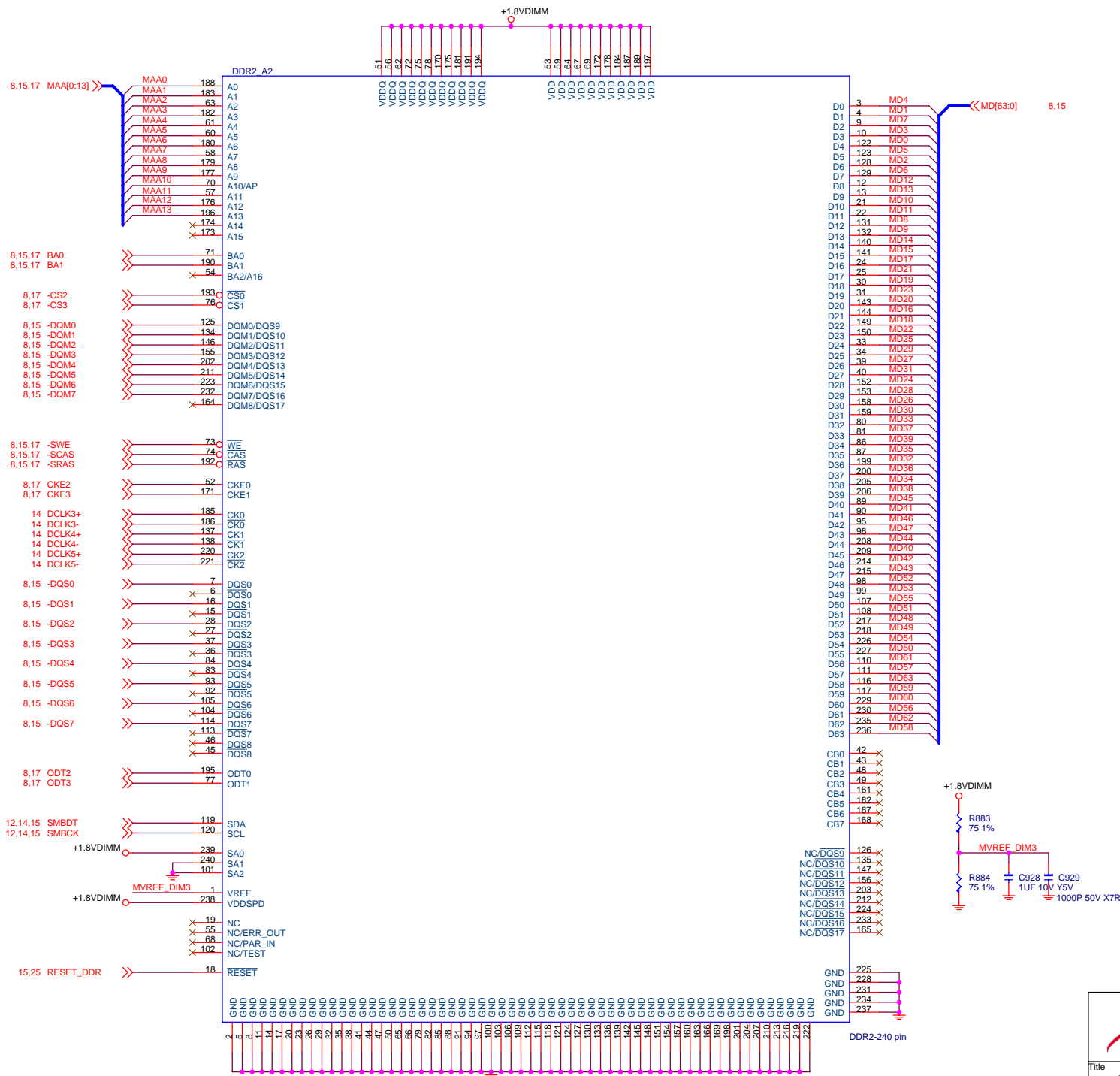
ICS950952

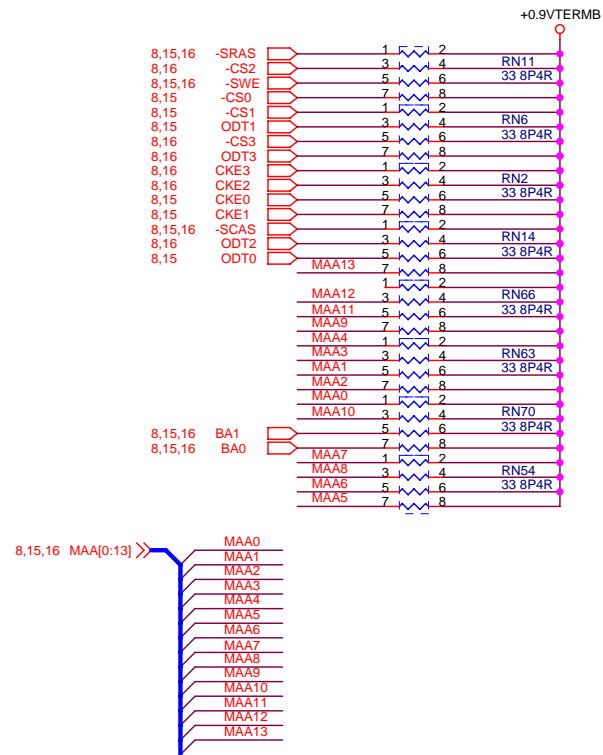
HCLK	C906	22P 50V NPO	NI
-HCLK	C907	22P 50V NPO	NI
CPU_CLK	C908	22P 50V NPO	NI
-CPU_CLK	C909	22P 50V NPO	NI
MCLK0-	C924	5P 50V NPO	NI
MCLK0+	C925	5P 50V NPO	NI
GCLK_NB	C994	22P 50V NPO	NI
GCLK_SLOT	C995	22P 50V NPO	NI
VCLK	C996	22P 50V NPO	NI
SPCLK	C997	22P 50V NPO	NI
APICCLK	C998	22P 50V NPO	NI
GUICLK	C999	22P 50V NPO	NI
SIO_OSC	C910	22P 50V NPO	NI
USBCLK	C911	22P 50V NPO	NI
LPCSIO_OSC	C890	22P 50V NPO	NI
AC97_CLK	C891	22P 50V NPO	NI

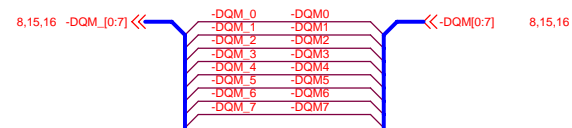
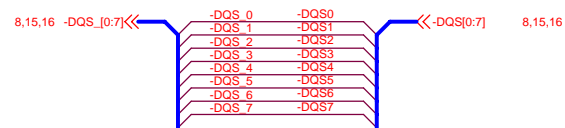
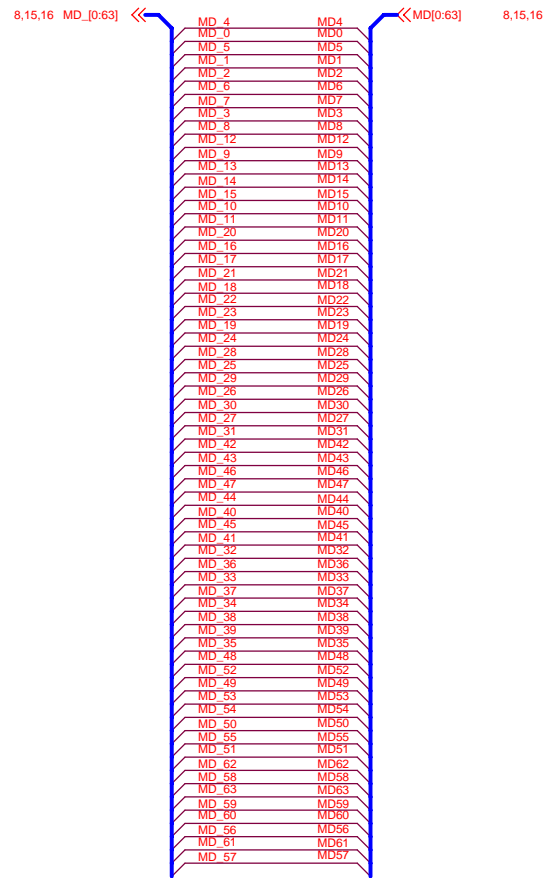


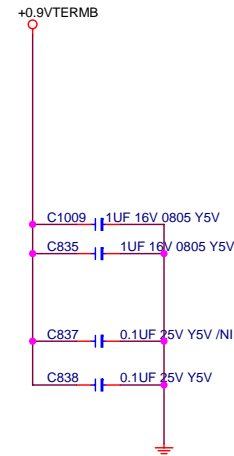
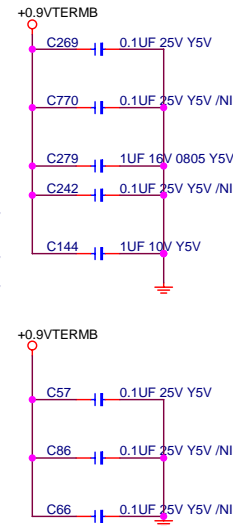
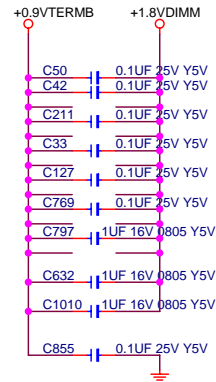
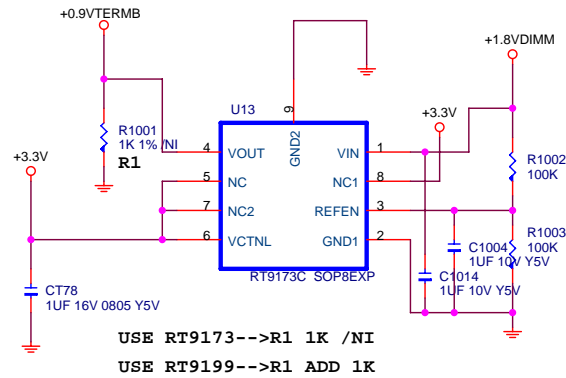
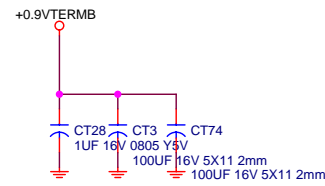


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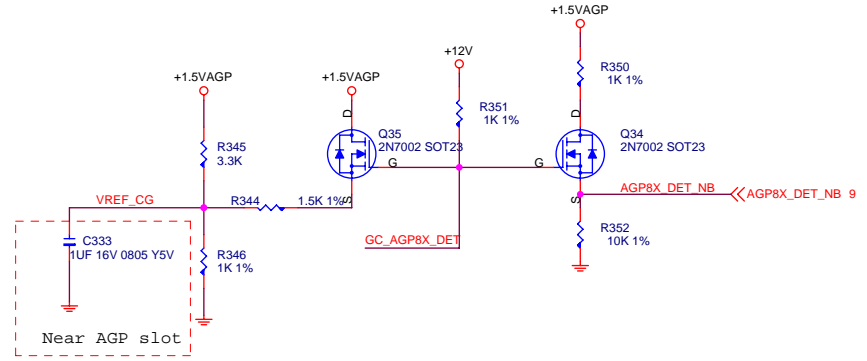
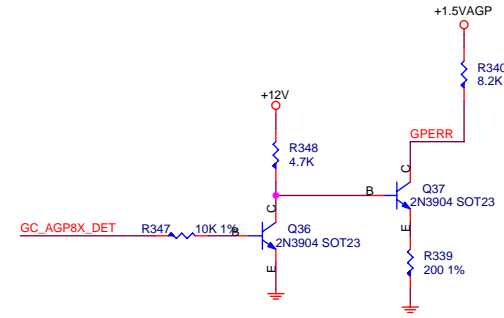
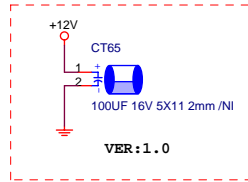
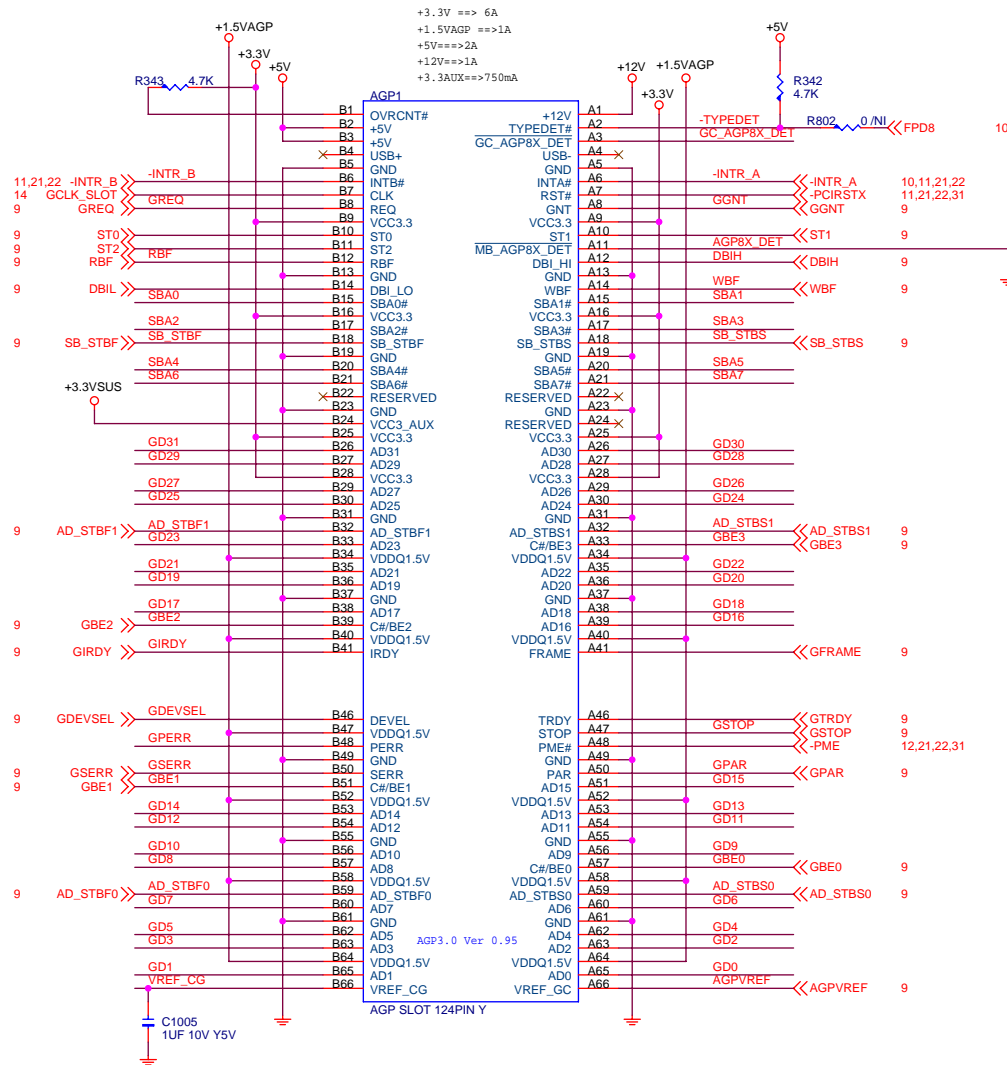


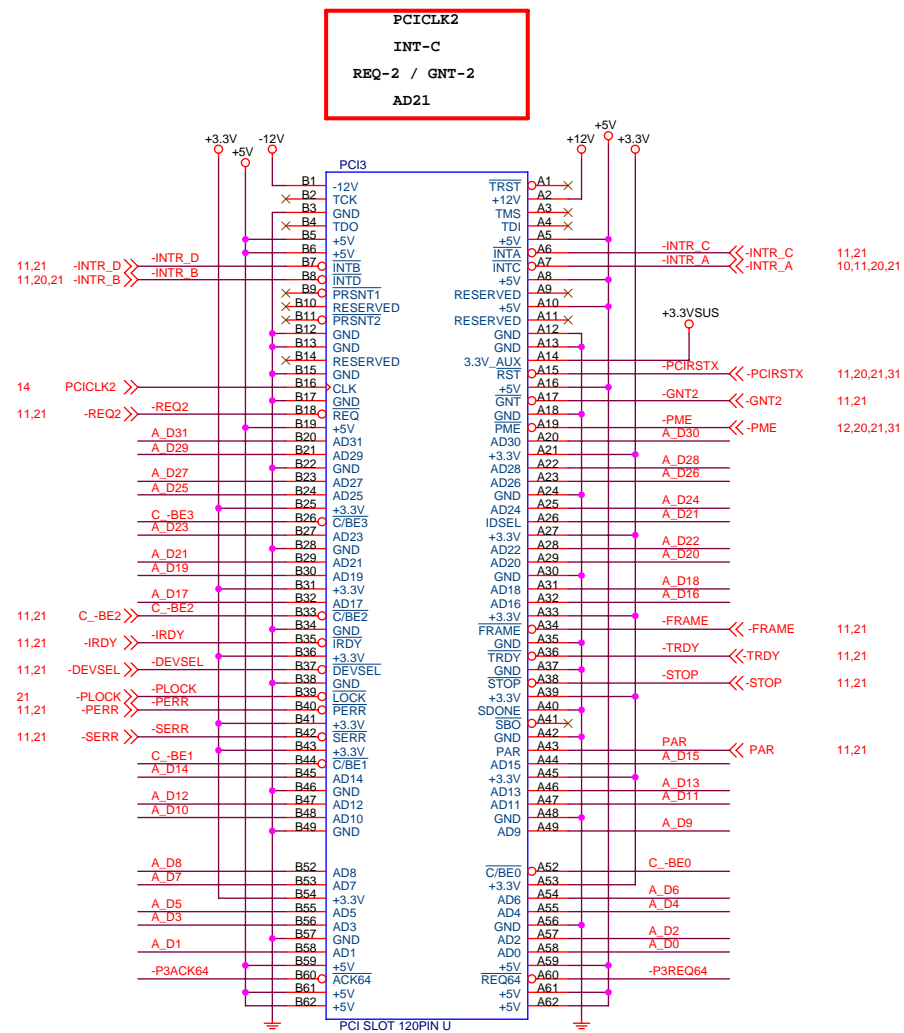






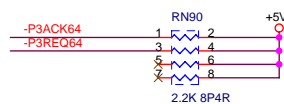
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9 GD[0:31] >> GD[0:31]

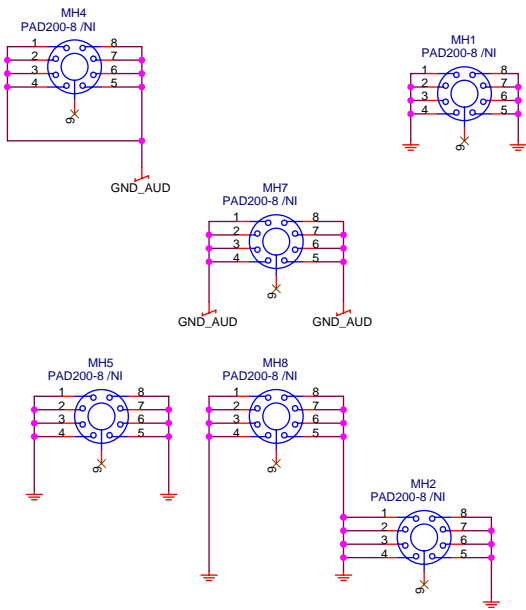




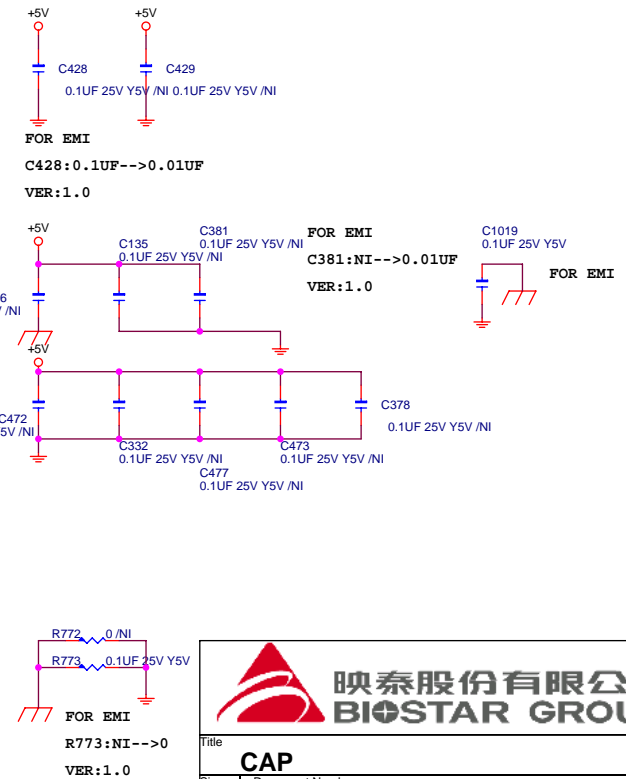
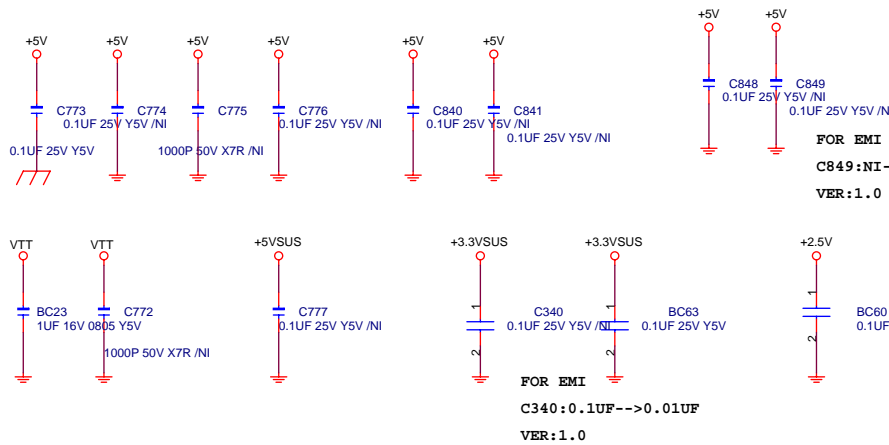
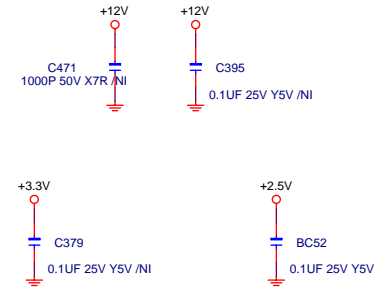
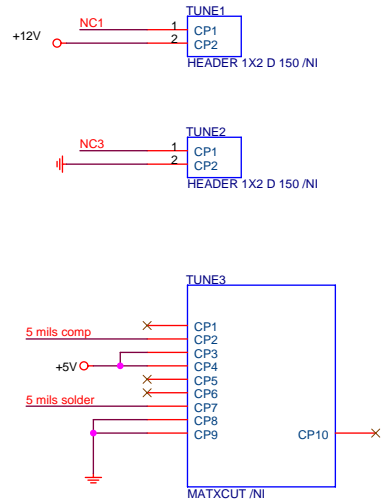
11,21 A_D[0..31] <<=====

11,21 C_-BE[0..3] >>=====





Impedance Testing Coupon



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Title
CAP

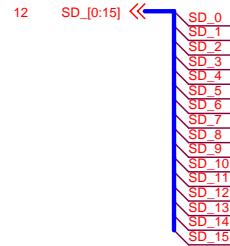
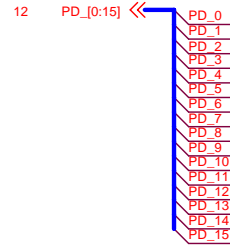
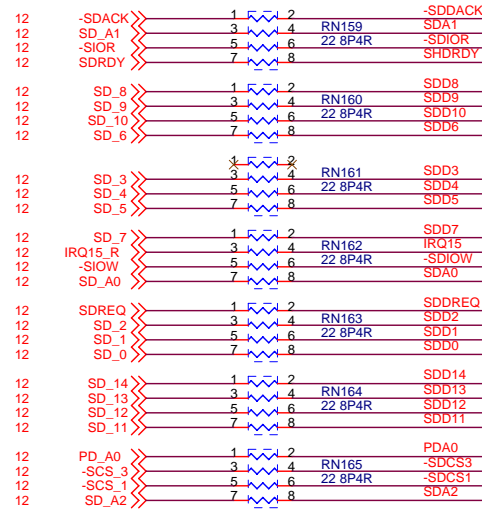
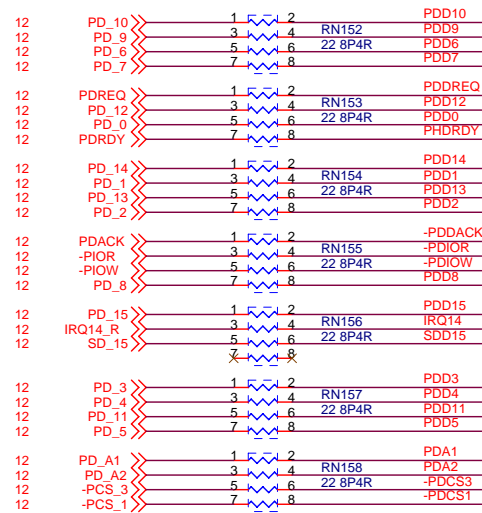
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Document Number
P4M8P-M7A

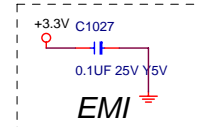
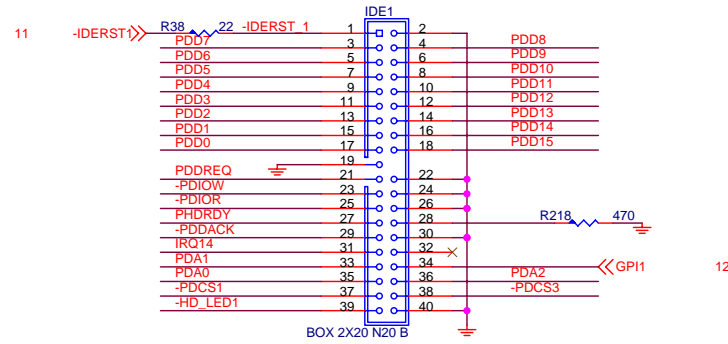
Rev
1.2

Date: Tuesday, April 18, 2006

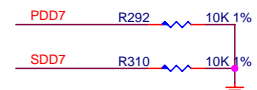
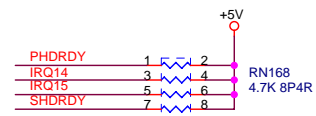
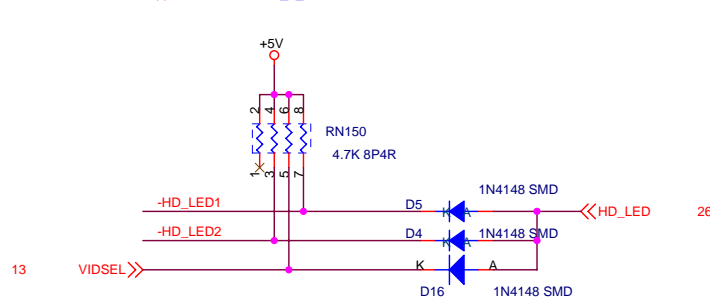
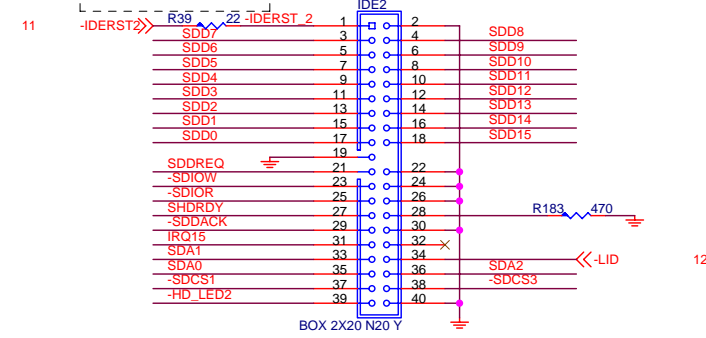
Sheet 23 of 36




PRIMARY



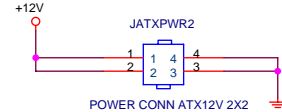
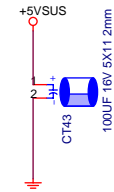
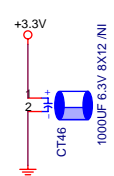
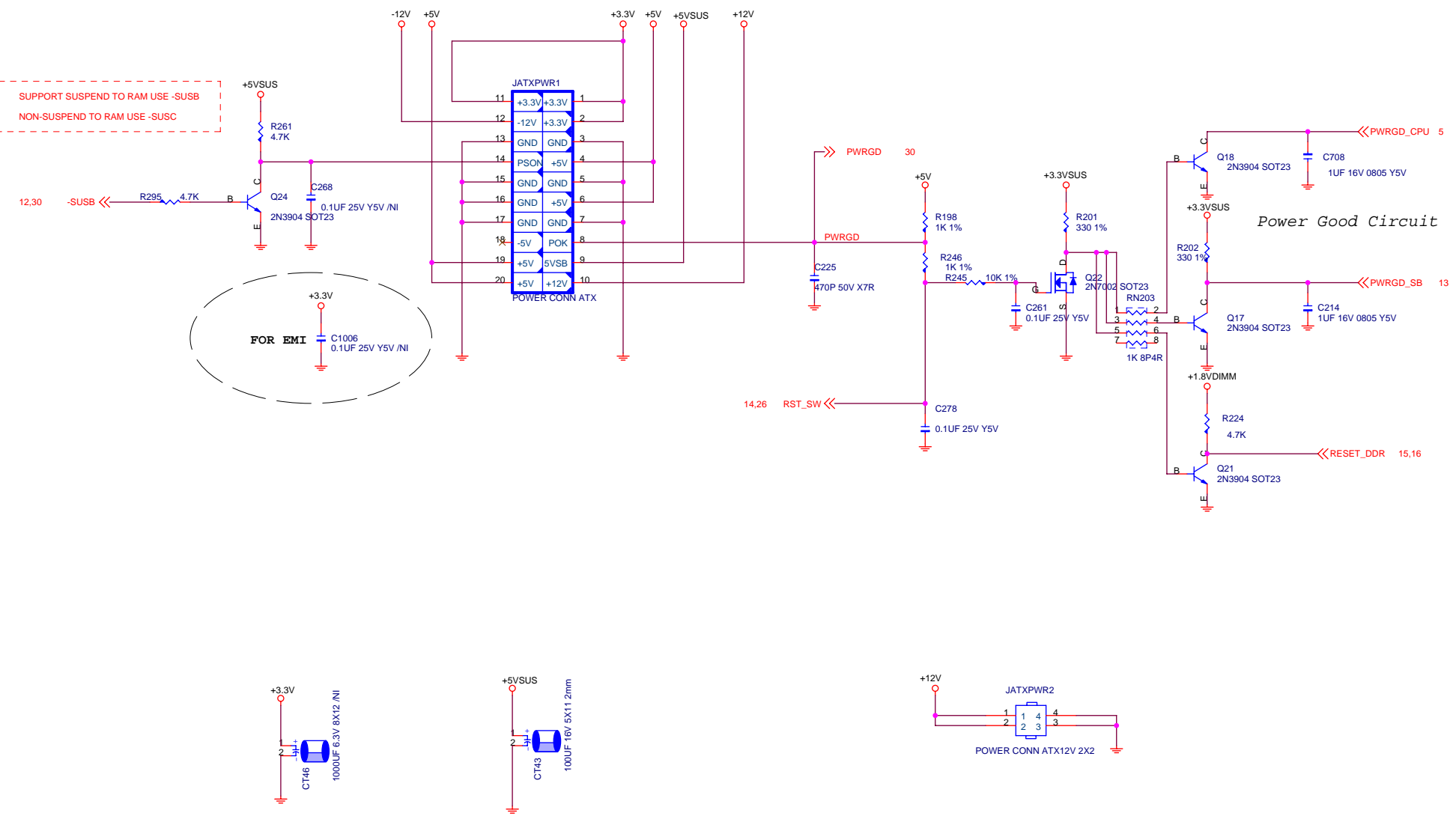
SECONDARY

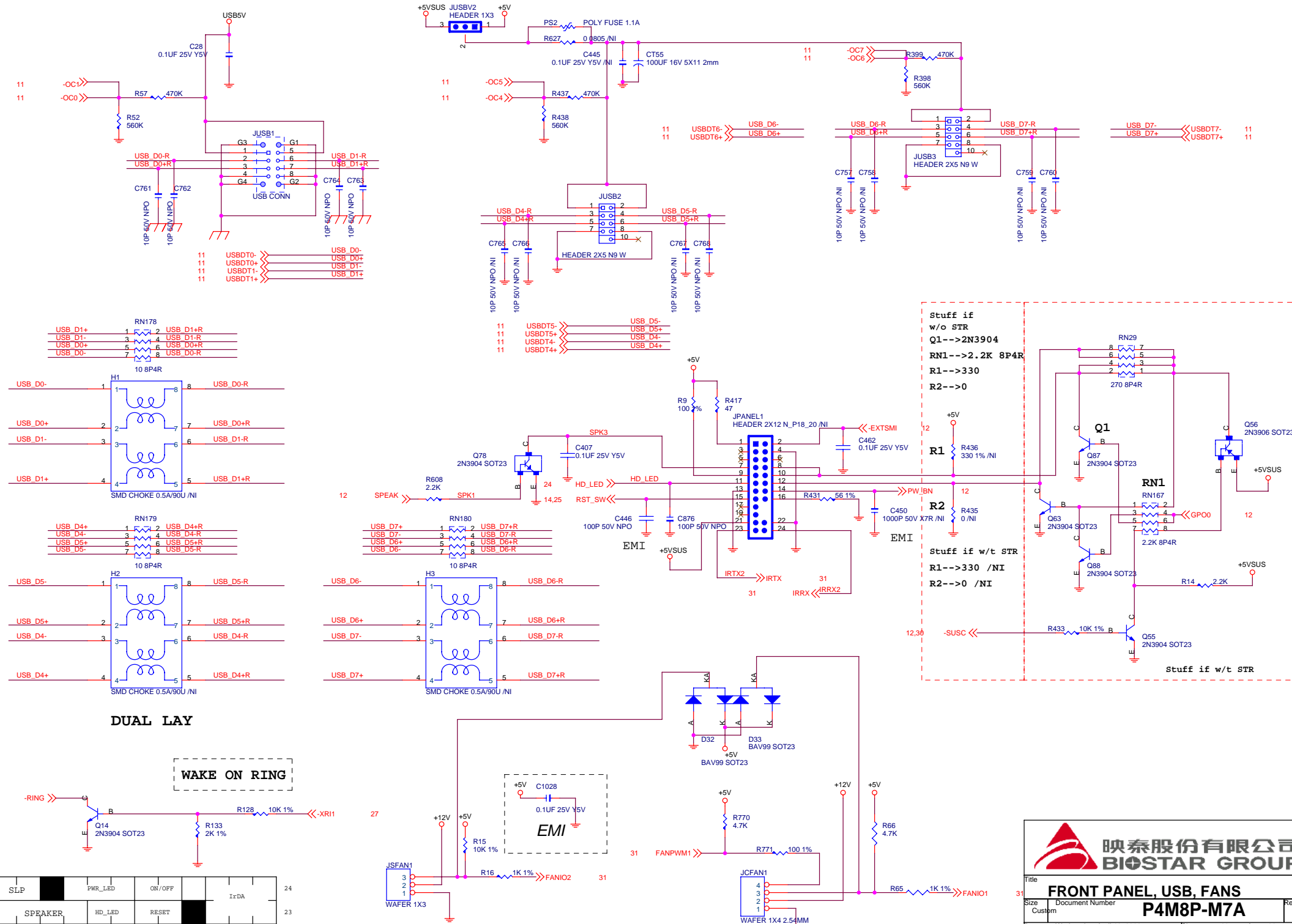




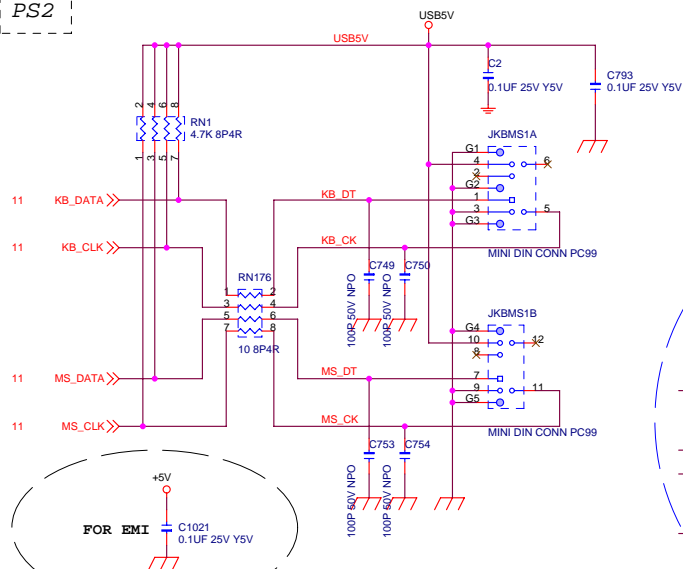
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Title IDE CONNECTOERS		
Size B	Document Number P4M8P-M7A	Rev 1.2
Date: Wednesday, April 19, 2006	Sheet 24	of 36

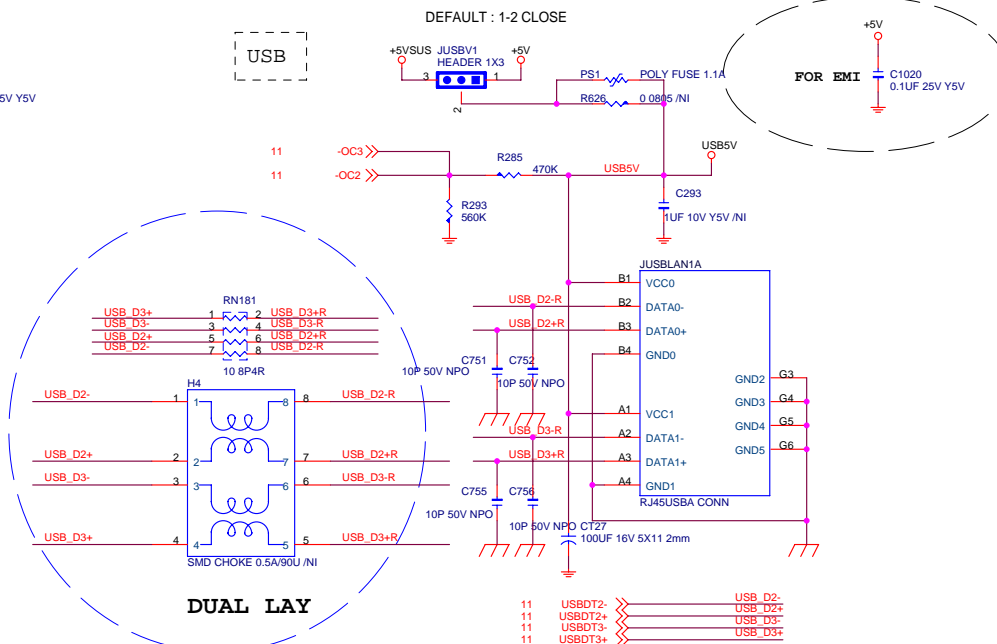




PS2

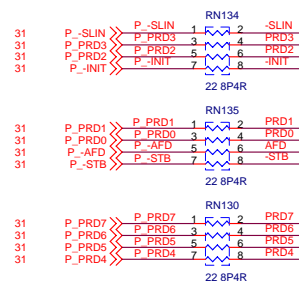
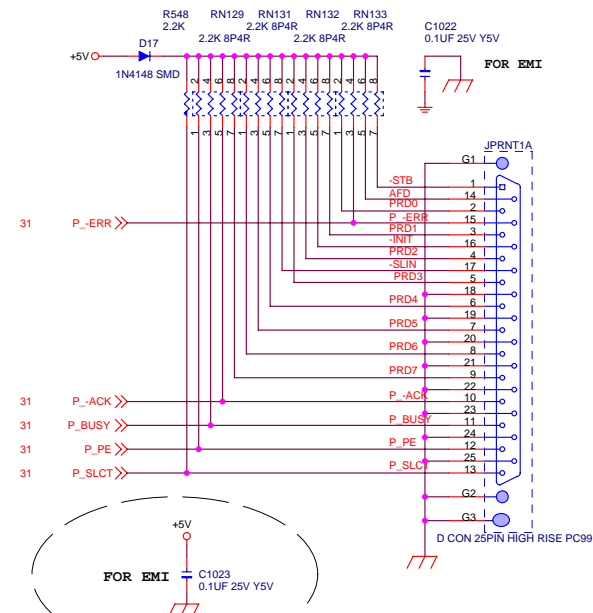
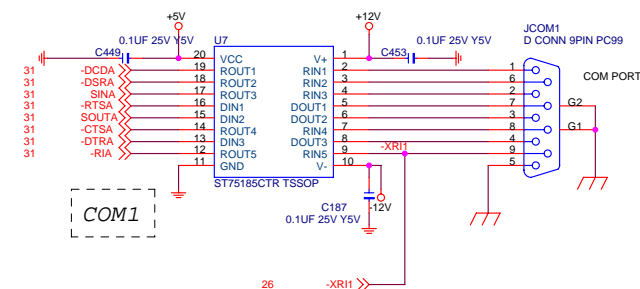


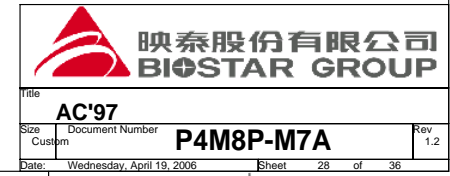
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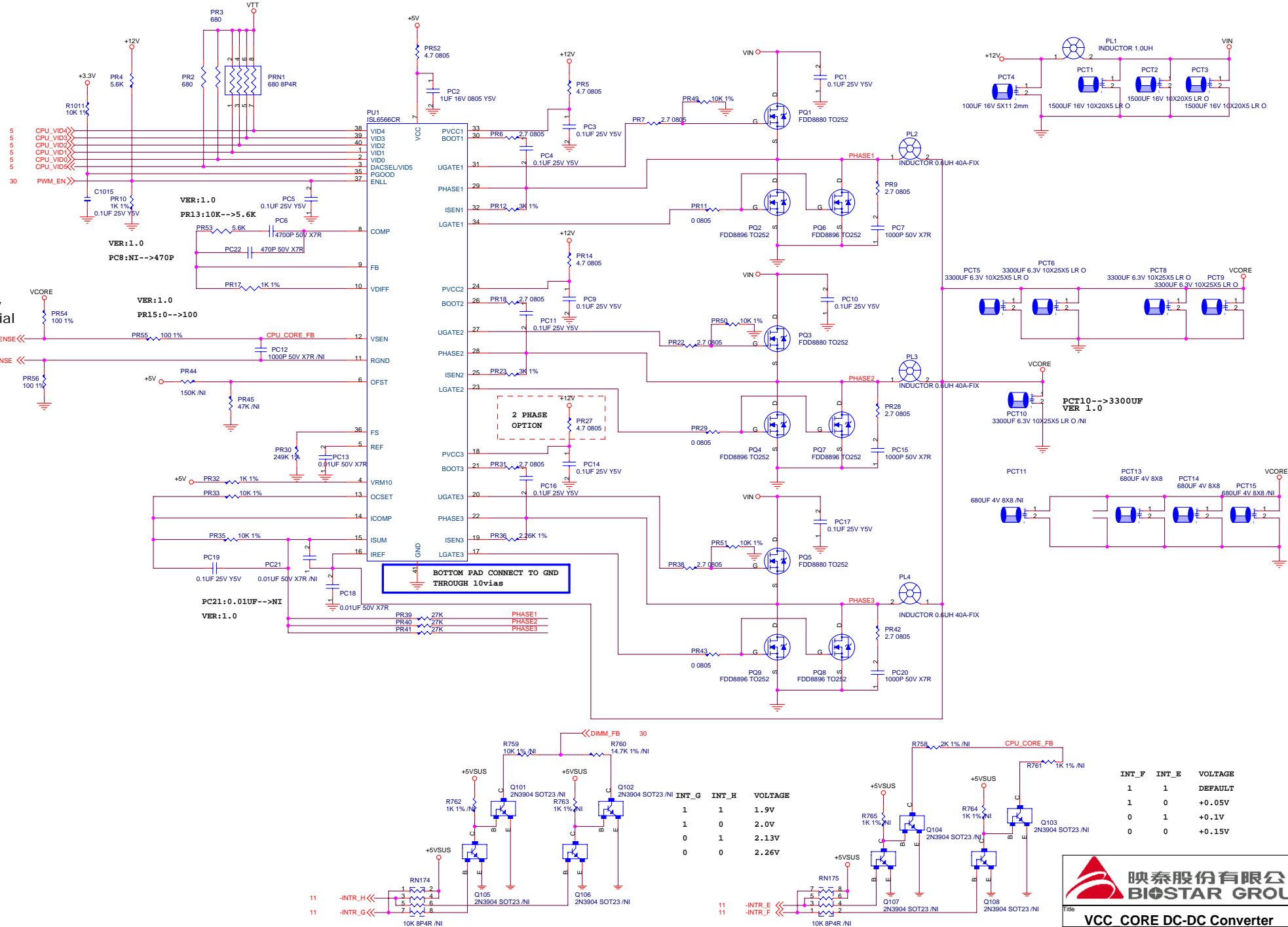
DUAL LAY

LPT





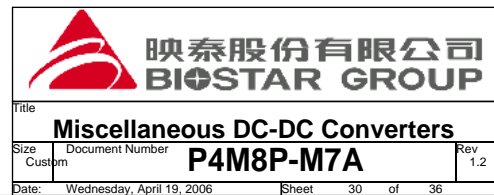
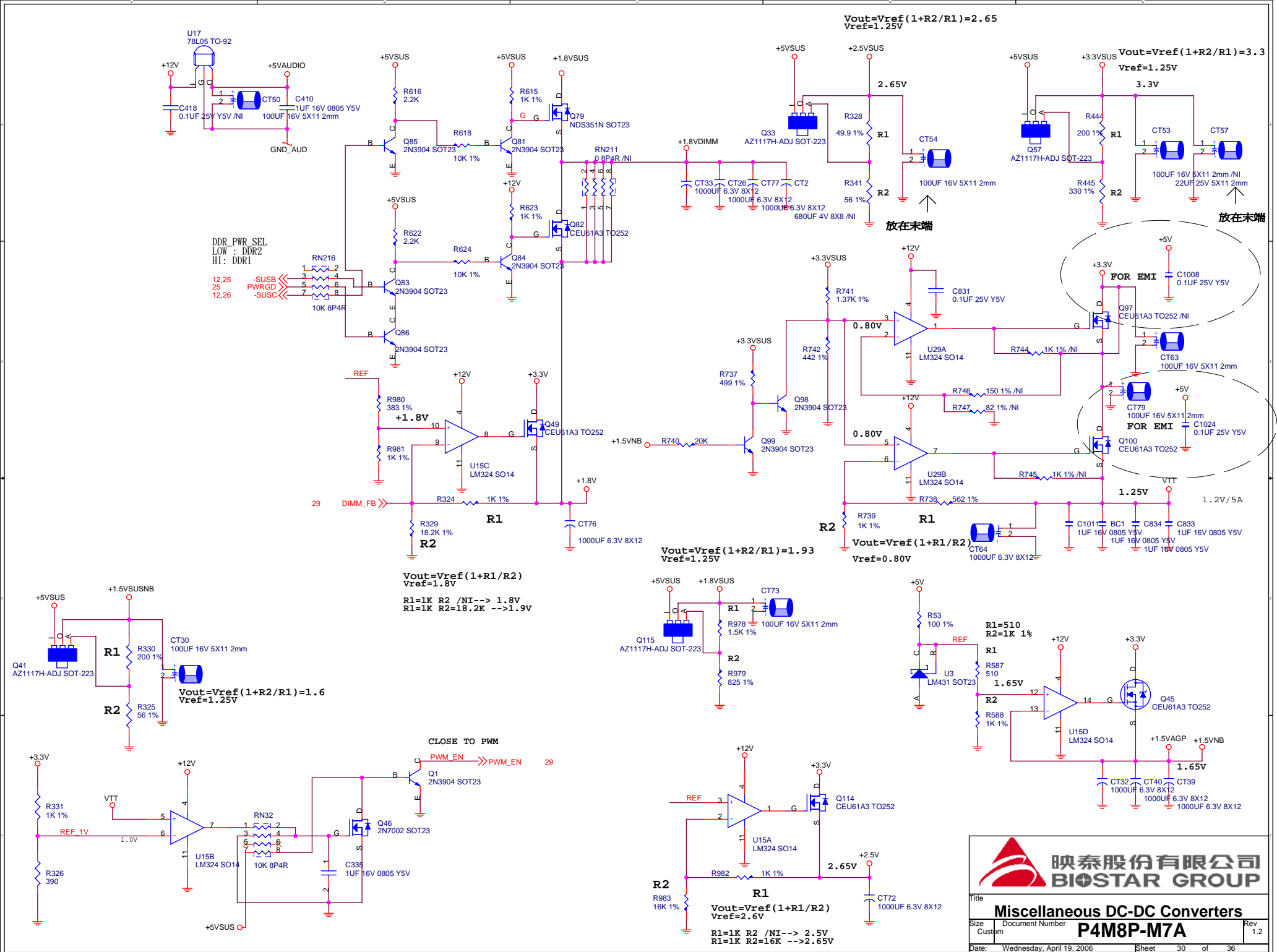
Route by
Differential



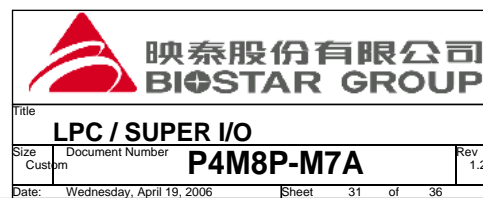
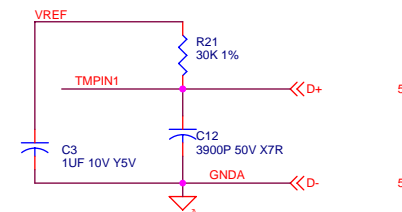
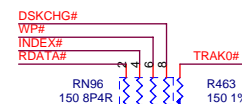
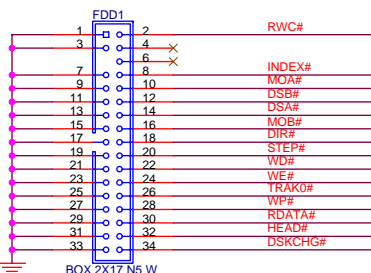
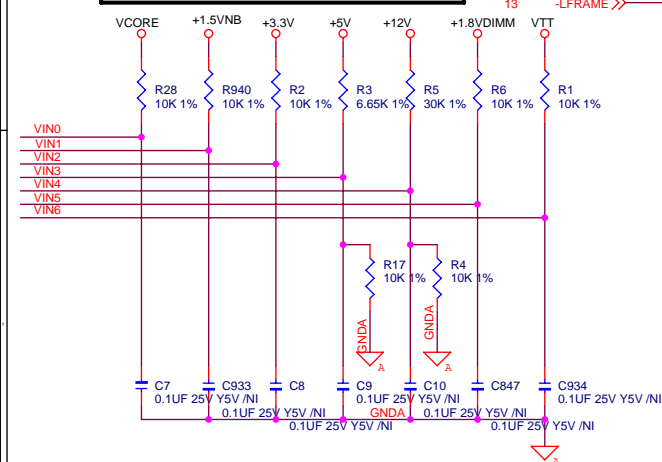
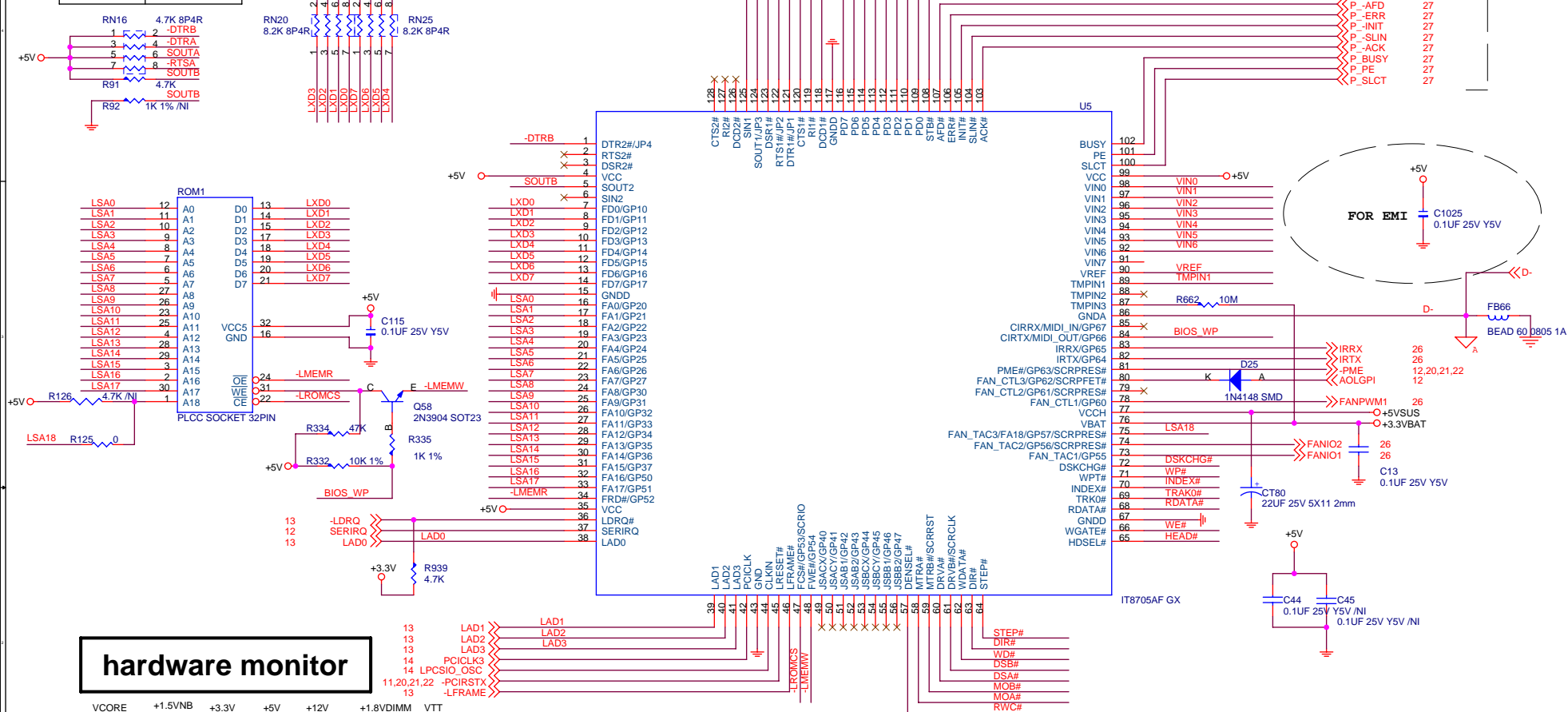
INT_F	INT_E	VOLTAGE
1	1	DEFAULT
1	0	+0.05V
0	1	+0.1V
0	0	+0.15V

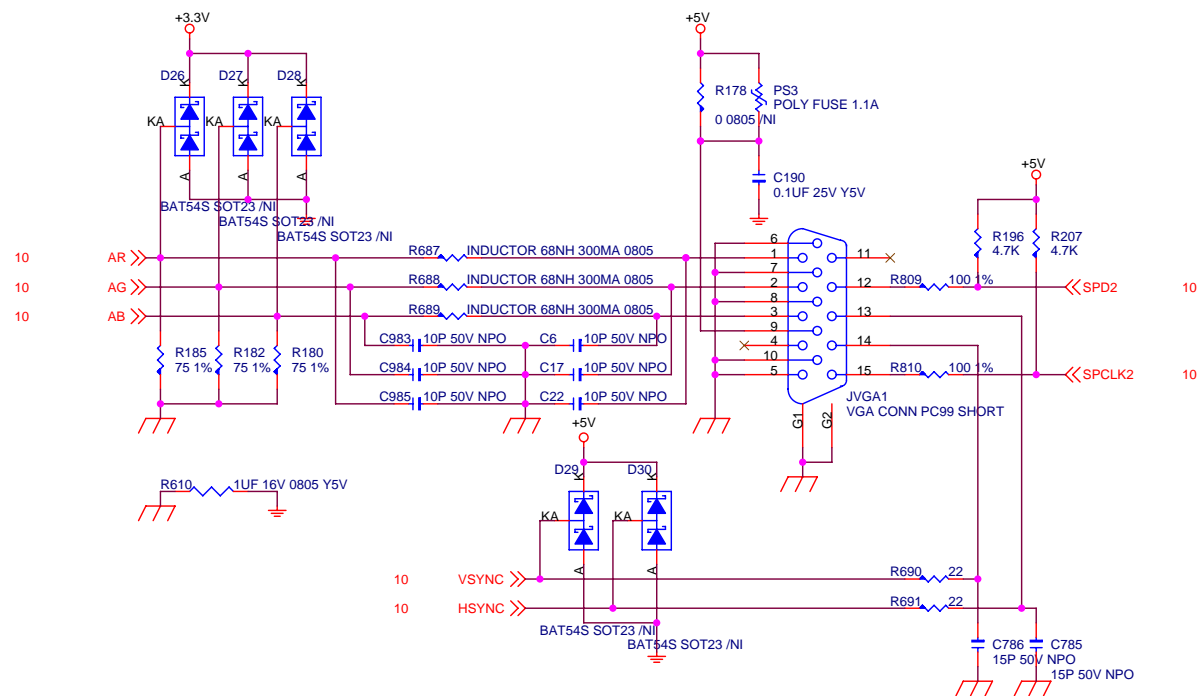


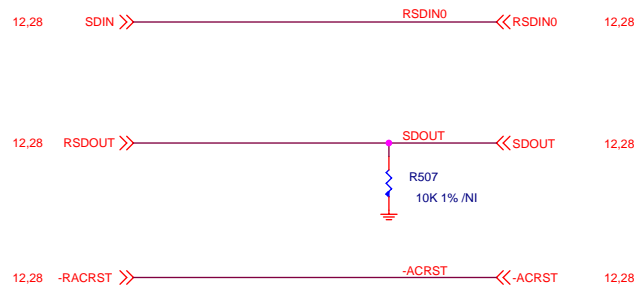
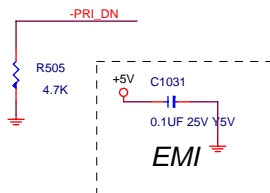
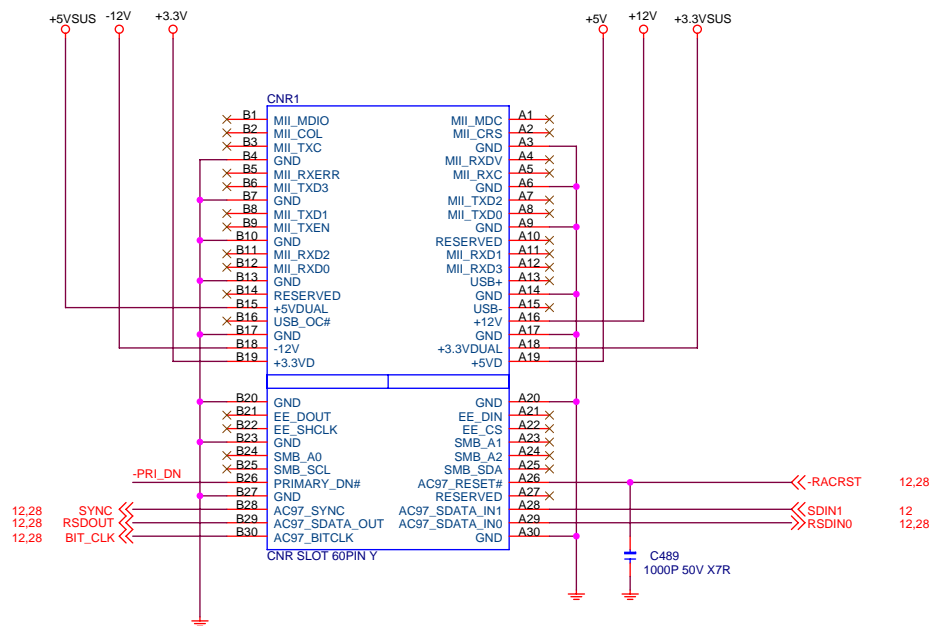
VCC CORE DC-DC Converter			Rev 1.2
Size	Document Number	P4M8P-M7A	
Date	Wednesday, April 19, 2006	Sheet 29 of 36	



ROM SIZE SELECT	
4M	2M
R91	R92







JUSBV1(1_2)
JUMPER 2P R

JUSBV2(1_2)
JUMPER 2P R

JFAUDIO1(5_6)
JUMPER 2P B

JFAUDIO1(9_10)
JUMPER 2P B

JFAUDIO1(11_12)
JUMPER 2P B

JFAUDIO1(13_14)
JUMPER 2P B

JCMOS1(1_2)
JUMPER 2P B

(BAT1)

電池

3V BATTERY SONY

(ROM1)

FLASH ROM

PLCC ISA 4M

PCB

PCB

P4M8P-M7 1.2

(PCB)

泡棉

POLON 245X200

(U11)

北橋散熱片

SBNP-S

(U18)

南橋散熱片

SBLV /NI

New JPANEL1 不含IR

JPANEL1 2*12

JPANEL1(2_4) JPANEL1(14_16)
HEADER 1X2 HEADER 1X2_3
JPANEL1(6_8_10_12)
PLED

JPANEL1(19_24)
IR /NI

JPANEL1(1_3_5_7) JPANEL1(13_15)
SPK JPANEL1(9_11)
HLED RST_3